REMARKS

Claims 1-4 are withdrawn. Claim 5 is amended. Claims 5-13 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendment and the following remarks.

I. Claims Rejected Under 35 U.S.C. § 103(a)

A. Claims 5, 12, and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes (U.S. Pre-Grant Publication No. 2001/0012225) in view of El Gamal et al. (U.S. Patent No. 6,642,543) and Huang et al. (U.S. Patent No. 6,146,795). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art. Among other elements, amended Clam 5 recites:

> "a).... a pixel array having a number of pixels, each pixel containing a drive transistor, a select transistor, a transfer transistor and a reset transistor;....
> g) forming a plurality of photodiodes and a plurality of the drive transistors, the select transistors, the transfer transistors and the reset transistors in the pixel array based on the first and the second gate insulator layers wherein all transistors of the pixel array have the first and the second gate insulator layers; and
> h) forming at least one transistor in the logic circuit based on the second gate insulator layer." (Emphasis added)

Applicants submit that the cited references, separately or in combination, do not teach or suggest these elements.

Rhodes discloses an image sensor having a pixel 14 containing a drive transistor 36, a select transistor 38, a transfer transistor 28, and a reset transistor 32. Rhodes also discloses a readout circuit 60 which may be characterized as the logic circuit. The Examiner relies on El Gamal for disclosing pixel transistors 510 and 520 in a thick gate region and a logic circuit comprising transistors 540 and 550 in a thin gate region (FIG. 5 of El Gamal). The Examiner also relies on El Gamal for disclosing transfer transistor 620 and reset transistor 630 located in a

thick gate region and thin gate transistors 640, 650, and 660 forming a logic circuit outside of the thick gate region (FIG. 6 of El Gamal). Huang is relied on for disclosing making thick gates by forming a second gate layer over a first gate layer, and making thin gates by forming the second layer over bare silicon.

However, the cited references, separately or in combination, do not teach or suggest that "all transistors of the pixel array have the first and the second gate insulator layers." By comparing FIG. 1 of Rhodes with FIGs. 5-6 of El Gamal, a skilled person in the art would understand that El Gamal's source follower transistors 510 and 640 correspond to Rhodes' drive transistors 36, which is part of the claimed pixel. Further, El Gamal's transistors 540 and 650 correspond to Rhodes' select transistor 38, which is also part of the claimed pixel. Thus, El Gamal discloses in both FIG. 5 and FIG. 6 that the select transistor (540, 650) is located in a thin gate region. Combining the teaching of Huang which discloses that a thin gate region may be formed by a second gate layer over bare silicon, a skilled person would understand that at least one of the pixel transistors (the select transistor) is formed on a thin gate layer (the second gate insulator layer). By contrast, the claimed method requires that all transistors of the pixel array have the first and the second gate insulator layers. Thus, the cited references at most teach or suggest some of the pixel transistors are based on a thick gate layer (the first and the second gate insulator layers). Nowhere in the cited references teach or suggest that all of the pixel transistors are based on a thick gate layer.

In addition to the select transistor, El Gamal also discloses that drive transistor (510, 640) which is part of the claimed pixel, may or may not be based on a thick gate. FIG. 5 of El Gamal shows that drive transistor 510 is within the thick gate region. FIG. 6 of El Gamal shows that drive transistor 640 is outside of the thick gate region. In the advisory action, the Examiner points to drive transistor 510 as a pixel transistor but then points drive transistor 640 as part of a logic circuit. Applicants submit that the transistor performing the same function may not be deemed as part of the pixel in one example and not part of the pixel in another example.

Moreover, El Gamal specifically discloses that thin oxide transistors are used wherever possible, and thick gate oxide transistors are used to ensure low leakage current and higher voltage swing (col. 4, lines 54-58). Nowhere does El Gamal teach or suggest that all of the pixel

transistors should be based on a thick gate. As mentioned above, Rhodes and Huang also fail to teach or suggest that "all transistors of the pixel array have the first and the second gate insulator layers." Thus, none of the cited references, separately or combined, teach or suggest all of the elements of Claim 5.

Claims 12 and 13 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 5, 12, and 13 are request.

B. Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes in view of El Gamal and Huang as applied to Claim 5 above, and further in view of Ahn (U.S. Patent No. 5,804,491). Applicants respectfully traverse the rejection.

Claims 7-9 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims.

The Examiner cites Ahn for disclosing a method of removing a gate insulator by wet etching with HF or BOE. However, Ahn does not cure the deficiency of Rhodes, El Gamal, and Huang for failing to teach that all transistors of the pixel array have the first and the second gate insulator layers. Thus, none of the cited references teach or suggest each of the elements of Claims 7-9. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 7-9 are requested.

C. Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes in view of El Gamal and Huang as applied to Claim 5 above, and further in view of Hori et al. (U.S. Patent No. 5,707,487). Applicants respectfully traverse the rejection.

Claims 10 and 11 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims.

The Examiner cites Hori for disclosing a method of removing a mask using sulfuric acid or an O2 plasma etch. However, Hori does not cure the deficiency of Rhodes, El Gamal, and Huang for failing to teach that all transistors of the pixel array have the first and the second gate insulator layers. Thus, none of the cited references teach or suggest each of the elements of Claims 10 and 11. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 10 and 11 are requested.

II. Allowable Subject Matter

Applicants note with appreciation the Examiner's indication that Claim 6 would be allowable if rewritten in independent form. Applicants respectfully submit that the amendment to Claim 5 has obviated the need to rewrite Claim 6. As Claim 5 is in condition for allowance, Claim 6 is allowable at least for the reasons mentioned in regard to Claim 5. Accordingly, reconsideration and withdrawal of the objection of Claim 6 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentability define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Eric S. Hyman, Reg. No. 30,139

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
Telephone (310) 207-3800
Facsimile (310) 820-5988

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Suzanne Johnston — 4/28/06 Date